Claims

We claim:

1. An electronic structure, comprising:

an internally circuitized substrate having a metallic plane on a first surface of the substrate; and

a redistribution structure having N dielectric layers, N metal planes, and a microvia structure through the N dielectric layers, wherein N is at least 2, wherein dielectric layer 1 is on the first surface of the substrate and on the metallic plane, wherein metal plane J is on dielectric layer J for J =1, 2, ..., N, wherein dielectric layer I is on dielectric layer I-1 and on metal layer I-1 for I = 2, ..., N, and wherein the microvia structure electrically couples metal plane N to the metallic plane.

2. The electronic structure of claim 1, wherein the microvia structure includes N microvias, wherein the microvia K passes through dielectric layer K for K = 1, 2, ..., N, wherein metal plane N is electrically coupled to microvia N, wherein metal plane J-1 electrically couples microvia J to microvia J-1 for J = 2, 3, ..., N, and wherein microvia 1 is electrically coupled to the metallic plane.

3. The electronic structure of claim 1, wherein the microvia structure includes a microvia that passes through the N dielectric layers, wherein the microvia electrically couples metal plane N to the metallic plane.

4. The electronic structure of claim 1, wherein the microvia structure includes a first microvia, wherein the first microvia passes through dielectric layers M through N, wherein M is at least 2, wherein N is at least 3, wherein M is less than N, and wherein metal plane N is electrically coupled to the first microvia.

5. The electronic structure of claim 4, wherein the microvia structure further includes a second microvia that passes through dielectric layers 1 through M-1, wherein metal plane M-1 electrically couples the first microvia to the second microvia, and wherein the second microvia is electrically coupled to the metallic plane.

6. The electronic structure of claim 4, wherein the microvia structure further includes M-1 second microvias, and wherein the second microvia K passes through dielectric layer K for K = 1, 2, ..., M-1, wherein the metal plane M-1 electrically couples the first microvia to second microvia M-1, wherein if M > 2 then metal plane J-1 electrically couples second microvia J to second microvia J-1 for J = 2, 3, ..., M-1, and wherein second microvia 1 is electrically coupled to the metallic plane.

7. The electronic structure of claim 1, wherein N = 2 or N = 3.

8. The electronic structure of claim 1, wherein the N dielectric layers each include a dielectric material having a stiffness of at least about 700,000 psi.

9. The electronic structure of claim 1, wherein the N dielectric layers each include a dielectric material having a glass transition temperature of at least about 150 °C.

10. The electronic structure of claim 1, wherein the N dielectric layers each include a dielectric material having a coefficient of thermal expansion of no more than about 50 ppm/°C.

11. The electronic structure of claim 1, wherein at least one of the metallic plane and the N metal planes includes a signal plane.

12. The electronic structure of claim 1, wherein at least one of the N metal planes includes a power plane.

13. The electronic structure of claim 1, wherein at least one of the N metal planes includes a ground plane.

14. The electronic structure of claim 1, wherein the substrate includes a dielectric material comprising a polytetrafluoroetheylene (PTFE) having silicon particles therein.

15. The electronic structure of claim 14, wherein the substrate further includes a ground plane, a power plane, and a signal plane, wherein the ground plane, the power plane, and the signal plane are each embedded within the dielectric material, and wherein the signal plane is disposed between the ground plane and the power plane.

16. The electronic structure of claim 14, wherein the substrate further includes a ground plane, first and second power planes, and first and second signal planes, wherein the ground plane, the first and second power planes, and the first and second signal planes are each embedded within the dielectric material, wherein the first signal plane is disposed between the ground plane and the first power plane, and wherein the second signal plane is disposed between the ground plane and the second power plane.

17. The electronic structure of claim 1, further comprising an electronic device electrically coupled to the metal plane N by a solder member.

18. The electronic structure of claim 17, wherein the electronic device includes a semiconductor chip.

19. The electronic structure of claim 17, wherein the electronic structure includes at least one power plane, and wherein a thickness of the redistribution layer is large enough that a nearest distance between the solder member and any power plane of the at least one power plane is not less than a predetermined minimum distance value.

20. The electronic structure of claim 19, wherein the predetermined minimum distance value is predetermined by requirements of a given radio frequency application.

21. The electronic structure of claim 1, wherein a plated through hole (PTH) passes through the substrate from the first surface to a second surface of the substrate, and wherein the metallic plane is electrically coupled to the PTH.

22. The electronic structure of claim 21, further comprising a second metallic plane on the second surface of the substrate and a second redistribution structure having P second dielectric layers, P second metal planes, and a second microvia structure through the P second dielectric layers, wherein P is at least 1, wherein second dielectric layer 1 is on the second surface of the substrate and on the second metallic plane, wherein second metal plane J is on second dielectric layer J for J =1, 2, ..., P, wherein if I > 1 then second dielectric layer I is on second dielectric layer I-1 and on second metal layer I-1 for I = 2, ..., P, wherein the microvia structure electrically couples the second metal plane P to the second metallic plane, and wherein the second metallic plane is electrically coupled to the PTH.

23. The electronic structure of claim 22, wherein P = N.

24. The electronic structure of claim 22, further comprising an electronic board electrically coupled to the second metal plane N by a solder member.

25. The electronic structure of claim 24, wherein the electronic board includes a circuit card.

26. A method for forming an electronic structure, comprising:

providing an internally circuitized substrate having a metallic plane on a first surface of the substrate; and

forming a redistribution structure including forming N dielectric layers, forming N metal planes, and forming a microvia structure through the N dielectric layers such that the microvia structure electrically couples metal plane N to the metallic plane, wherein N is at least 2, and wherein forming the N dielectric layers and the N metal layers includes setting a dummy index J=0 and looping over J as follows:

adding 1 to J;

if J = 1 then forming dielectric layer 1 on the first surface of the substrate and on the metallic plane, else forming dielectric layer J on dielectric layer J-1 and on metal plane J-1;

forming metal plane J on dielectric layer J; and

if $J < N$ then returning to adding 1 to J and continuing the looping, else ending the looping.

27. The electronic structure of claim 26, wherein forming the microvia structure includes forming N microvias, wherein the microvia K passes through dielectric layer K for K = 1, 2, ..., N, wherein metal plane N is electrically coupled to microvia N, wherein metal plane J-1 electrically couples microvia J to microvia J-1 for J = 2, 3, ..., N, and wherein microvia 1 is electrically coupled to the metallic plane.

28. The method of claim 26, wherein forming the microvia structure includes forming a microvia that passes through the N dielectric layers, wherein the microvia electrically couples metal plane N to the metallic plane.

29. The method of claim 26, wherein forming the microvia structure includes forming a first microvia, wherein the first microvia passes through dielectric layers M through N, wherein M is at least 2, wherein N is at least 3, and wherein M is less than N, wherein metal plane N is electrically coupled to the first microvia.

30. The method of claim 29, wherein forming the microvia structure further includes forming a second microvia that passes through dielectric layers 1 through M-1, wherein metal plane M-1 electrically couples the first microvia to the second microvia, and wherein the second microvia is electrically coupled to the metallic plane.

31. The method of claim 29, wherein forming the microvia structure further includes forming M-1 second microvias, and wherein the second microvia K passes through dielectric layer K for K = 1, 2, ..., M-1, wherein the metal plane M-1 electrically couples the first microvia to second microvia M-1, wherein if M > 2 then metal plane J-1 electrically couples second microvia J to second microvia J-1 for J = 2, 3, ..., M-1, and wherein second microvia 1 is electrically coupled to the metallic plane.

32. The method of claim 26, wherein N = 2 or N = 3.

33. The method of claim 26, wherein the N dielectric layers each include a dielectric material having a stiffness of at least about 700,000 psi.

34. The method of claim 26, wherein the N dielectric layers each include a dielectric material having a glass transition temperature of at least about 150 °C.

35. The method of claim 26, wherein the N dielectric layers each include a dielectric material having a coefficient of thermal expansion of no more than about 50 ppm/°C.

36. The method of claim 26, wherein at least one of the metallic plane and the N metal planes includes a signal plane.

37. The method of claim 26, wherein at least one of the N metal planes includes a power plane.

38. The method of claim 26, wherein at least one of the N metal planes includes a ground plane.

39. The method of claim 26, wherein the substrate includes a dielectric material comprising a polytetrafluoroetheylene (PTFE) having silicon particles therein.

40. The method of claim 39, wherein the substrate further includes a ground plane, a power plane, and a signal plane, wherein the ground plane, the power plane, and the signal plane are each embedded within the dielectric material, and wherein the signal plane is disposed between the ground plane and the power plane.

41. The method of claim 39, wherein the substrate further includes a ground plane, first and second power planes, and first and second signal planes, wherein the ground plane, the first and second power planes, and the first and second signal planes are each embedded within the dielectric material, wherein the first signal plane is disposed between the ground plane and the first power plane, and wherein the second signal plane is disposed between the ground plane and the second power plane.

42. The method of claim 26, further comprising electrically coupling an electronic device to the metal plane N by a solder member.

43. The method of claim 42, wherein the electronic device includes a semiconductor chip.

44. The method of claim 42, wherein the electronic structure includes at least one power plane, and further comprising predetermining a minimum distance value, wherein forming the redistribution layer includes making a thickness of the redistribution layer large enough that a nearest distance between the solder member and any power plane of the at least one power plane

is not less than the predetermined minimum distance value.

45. The method of claim 44, wherein predetermining a minimum distance value includes utilizing requirements of a given radio frequency application.

46. The method of claim 26, further comprising forming a plated through hole (PTH) through the substrate from the first surface to a second surface of the substrate, and electrically coupling the metallic plane to the PTH.

47. The method of claim 46, further comprising forming a second metallic plane on a second surface of the substrate, electrically coupling the second metallic plane to the PTH, and forming a second redistribution structure including forming P second dielectric layers, forming P second metal planes, and forming a second microvia structure through the P second dielectric layers such that the second microvia structure electrically couples the second metal plane P to the second metallic plane, wherein P is at least 1, and wherein forming the P second dielectric layers and the P second metal layers includes setting a dummy index L=0 and looping over L as follows:

adding 1 to L;

if L = 1 then forming second dielectric layer 1 on the second surface of the substrate and on the second metallic plane, else if P > 1 then forming second dielectric layer L on second dielectric layer L-1 and on second metal plane L-1;

forming second metal plane L on second dielectric layer L; and

if L < P then returning to adding 1 to L and continuing the looping, else ending the looping.

48. The method of claim 47, wherein P = N.

49. The method of claim 47, further comprising electrically coupling an electronic board to the second metal plane N by a solder member.

50. The method of claim 49, wherein the electronic board includes a circuit card.